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**Thermal standardization on semiconductor packages –
Part 2-1: 3D thermal simulation models of semiconductor packages for steady-
state analysis – Discrete packages**

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INTERNATIONAL ELECTROTECHNICAL COMMISSION

THERMAL STANDARDIZATION ON SEMICONDUCTOR PACKAGES –**Part 2-1: 3D thermal simulation models of semiconductor packages for steady-state analysis – Discrete packages**

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The text of this International Standard is based on the following documents:

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The language used for the development of this International Standard is English.

This document was drafted in accordance with ISO/IEC Directives, Part 2, and developed in accordance with ISO/IEC Directives, Part 1 and ISO/IEC Directives, IEC Supplement, available at www.iec.ch/members_experts/refdocs. The main document types developed by IEC are described in greater detail at www.iec.ch/publications.

A list of all parts in the IEC 63378 series, published under the general title *Thermal standardization on semiconductor packages*, can be found on the IEC website.

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THERMAL STANDARDIZATION ON SEMICONDUCTOR PACKAGES –

Part 2-1: 3D thermal simulation models of semiconductor packages for steady-state analysis – Discrete packages

1 Scope

This part of IEC 63378 specifies three-dimensional (3D) thermal models of discrete semiconductor packages (TO-243, TO-252 and TO-263), utilized in the steady-state thermal analysis of electronic devices to estimate junction temperatures accurately.

This model is assumed to be made by semiconductor suppliers and to be used by assembly makers of electronic devices.

2 Normative references

There are no normative references in this document.